

## An introduction to depletion-mode MOSFETs

Planet Analog, 8/7/2006

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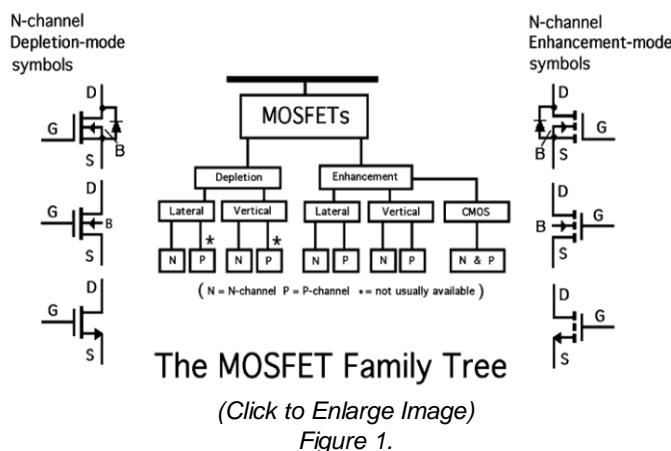
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Since the mid-nineteen seventies the "enhancement-mode" MOSFET has been the subject of almost continuous global research, development, and refinement by both the semiconductor industry and academia. As a result it has become the predominant MOSFET topology that encompasses discrete MOS power switches and CMOS. By contrast, the depletion-mode MOSFET has not received the same attention or popularity over this time, despite being the oldest member of the MOSFET family. It does have some rather unique characteristics though, which cannot be easily replicated by other means. This article will look at depletion mode MOSFET device structure, operation and applications to help designers further exploit some of the unique characteristics of these devices.

### Structure

The MOSFET transistor family consists of two main types, these being "depletion-mode" and "enhancement-mode" types. Although MOSFETs can be made in either polarity, N-channel MOSFETs are available in all four types while P-channel depletion-mode devices are not generally available. However, manufacturers sometimes create P-channel depletion devices during the manufacture of certain analog and digital ICs. In fact, depletion-mode transistors were commonly used in NMOS logic circuits until the clear advantages of CMOS became apparent. These advantages include increased circuit density, significantly lower power, and the ability to create analog and digital circuitry side-by-side on the same chip. The MOS family tree and its various (N-channel) symbols are shown in **Figure 1**.



Unlike enhancement-mode transistors, which are "normally-off" devices, depletion-mode MOSFETs are "normally-on". N-channel devices are built with P-type silicon substrates, and P-channel versions are built on N-type substrates. In both cases they include a thin gate oxide situated between the source and drain regions. A conductive channel is deliberately formed beneath the gate oxide layer and between the source and drain by using ion-implantation. By implanting the correct ion polarity in the channel region during manufacture determines the polarity of the threshold voltage (i.e.  $-V_{TH}$  for an N-channel transistor, or  $+V_{TH}$  for a P-channel transistor). The actual concentration of ions in

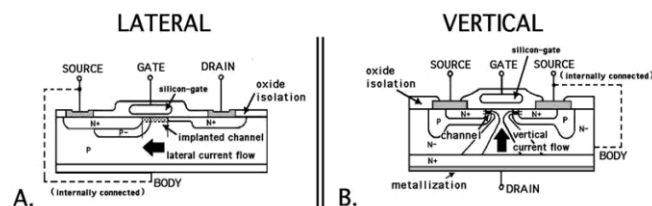
the substrate-to-channel region is used to adjust the threshold voltage ( $V_{TH}$ ) to the desired value. Depletion-mode devices are a little more difficult to manufacture and their characteristics harder to control than enhancement types, which do not require ion-implantation.

While their particular geometries are different, all FETs share the same terminal designations, i.e. "gate", "source", and "drain", but MOSFETs also have an extra terminal called the "body" (also known as "bulk" or "substrate"). For most practical purposes this can be considered as internally connected to the source (as is the case with CMOS devices and power MOSFETs). If the body terminal is available separately, then for N-channel devices it should be connected to the most negative point in the circuit, or for P-channel devices, to the most positive point.

A metal oxide semiconductor, or MOS transistor, has either a metal gate (an older technology), or more usually a polysilicon-gate (a newer technology), built on top of the insulating gate oxide. For a depletion-mode MOSFET the channel is fully conductive and current flows strongly between the drain and source when the gate terminal is at zero volts ( $V_{GS} = 0V$ ). An increasingly negative bias at the gate of an N-channel device will reduce conduction in the channel, until finally  $-V_{GS(off)}$ , the device's threshold voltage ( $V_{TH}$ ) is reached, and conduction ceases.

While the depletion-mode MOSFET shares some of the Junction FET's (JFET) operating characteristics it is constructed differently, and is quite similar to the enhancement-mode MOSFET. The structure of any MOS device dictates whether the current flows through it laterally (see **Figure 2a**), or vertically (see **Figure 2b**), and thereby the orientation of its channel. Typically the "lateral" structure has its drain, source, and gate terminals located on the top surface of the chip, which is more suitable for integration.

The lateral device has a horizontal channel, and offers some important advantages including a low forward capacitance; an ultra-fast turn-on speed; and thus a high operating frequency, which can typically reach several hundred megahertz. The lateral type is made by Advanced Linear Devices Inc., who offer matched dual and quad depletion-mode devices (i.e. ALD114804) using their proprietary EPAD' technology. Another lateral manufacturer is Philips Semiconductors of who make several discrete RF depletion-mode parts (i.e. BF1107 family).



The depletion-mode MOSFET can be built using either a lateral structure (shown in A), or a vertical structure (shown in B). The lateral structure is more suitable for integration and provides lower capacitance and higher speed, while the vertical structure supports higher breakdown voltage, lower on-resistance, and higher current capability. N-channel shown here.

(Click to Enlarge Image)  
Figure 2.

In comparison, the vertical structure, shown in Figure 2b, provides a lower on-resistance, and supports a significantly higher current capability. This structure is essential for power devices because the physical distance between source and drain regions must be quite large, in order to maintain a high voltage-blocking capability. A FET's drain-to-source current is inversely proportional to this distance. As shown in Figure 2b, a typical N-channel (DMOS) power FET is built with two separate diffusions to create its structure.

This is where the term "DMOS", meaning "Double-diffused MOS" transistor, originates. The medium- and high-power depletion-mode MOSFET has a higher level of breakdown voltage than either the JFET or many enhancement-mode devices. This is as low as 60-volts, but in some cases as high as 1,000-volts. Of the two kinds of structures used for

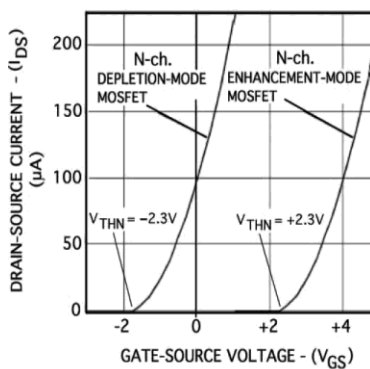
creating discrete depletion-mode MOSFETs, the vertical DMOS structure is the most commonly available type. It is made by Supertex Inc., Infineon Technologies Inc., Clare Inc., and IXYS Corp., summarized further below in **Table 2**.

## Operation

A major difference between the operation of any MOSFET and the bipolar junction transistor (BJT) is that the FET is voltage-controlled, whereas the BJT is current-controlled. To control current passing between the drain and the source of a FET one uses a control voltage at its gate. With the BJT, a combination of base voltage and base current is involved.

Being a depletion-mode device, this "normally-on" MOSFET type acts as a "normally-closed" (N.C., 1-Form-B) switch, and requires no gate current to function. The depletion-mode operates by applying a more negative gate voltage than the threshold voltage  $-V_{TH}$  or  $-V_{GS(off)}$ , which has the effect of "depleting" or shutting off the majority current carriers in the pre-formed channel beneath the gate. It does this by changing the size of the depletion region under the gate area, thus increasing the channel resistance and reducing the current flow. The cross-sectional area ( $L \times W$ ) of the MOSFET's channel is fixed by the device geometry.

However, the thickness and position of the channel is controlled by a combination of the gate-to-source voltage ( $V_{GS}$ ), and the drain-to-source voltage ( $V_{DS}$ ). These effectively change the resistance in the channel, allowing full, partial, or no conduction. A comparison between operation of an N-channel depletion-mode and enhancement-mode MOS devices is shown in **Figure 3**.



Comparing the transfer characteristics of Depletion-mode and Enhancement-mode N-channel devices.

[\(Click to Enlarge Image\)](#)

Figure 3.

The MOSFET is primarily a "transconductance" device where the input voltage and the output current are directly related, such that gate voltage ( $V_G$ ) is transferred to the source-drain current ( $I_{DS}$ ), and where  $G_m$  applies to its conductance. It is also a "unipolar" device because only one type of current carrier is utilized to support conduction (unlike the BJT which utilizes both electrons and holes). Because the MOSFET is a "majority-carrier" device it does not suffer from minority-carrier storage time effects like BJTs, thereby switching much faster. N-channel FETs utilize electrons that are negative carriers, whereas P-channel FETs use holes, which are positive carriers.

Because electrons have a higher mobility than holes, they move faster through the semiconductor crystal lattice. This higher speed capability translates into the fact that N-channel FETs of all types are more popular and more available than P-channel FETs. Generally the smaller the FET chip, the lower capacitance, and the faster, though less powerful, it will be.

Large MOSFET chips are designed for power switching, and have a much lower "on-resistance" -  $R_{ds(on)}$ , and thereby a higher current capability. They have higher input and output capacitances, and are therefore slower.

Medium-/high-power depletion-mode MOSFETs typically offer higher voltage operation than many enhancement types. While both JFETs and depletion-mode MOSFETs have a similar operating frequency range, in many cases the depletion-mode MOSFET is faster (over 400-MHz). **Table 1** shows the symbols, structures, and some important characteristics for depletion-mode MOSFETs.

A. MOSFET type:	B. Symbol & polarities	C. Cross-sectional view	D. Transfer characteristic	E. Output characteristic
N-channel Depletion-mode				
P-channel Depletion-mode				
Showing the symbols, architectures, and key characteristics for depletion-mode MOSFETs. Lateral devices are shown for simplicity. Note that for most MOSFETs the substrate or Body terminal is internally tied to the source terminal.				

(Click to Enlarge Image)  
Table 1.

## Practical considerations of depletion-mode MOSFETs

A completely unique feature of depletion-mode MOSFETs is that they can also be made to work in the "enhancement-mode". This is achieved by making the gate-to-source voltage ( $V_{GS}$ ), slightly positive by a volt or two for N-channel, or slightly negative by a volt or two for P-channel devices. This allows increased current levels beyond the normal  $I_{DSS}$  point, as seen in **Table 1d**. Because the depletion-mode MOSFET has an insulated capacitive gate (not a gate-channel diode like the JFET), this reverse-bias condition is quite acceptable so long as the breakdown voltage rating is not exceeded. Depletion-mode MOSFETs share many of the same characteristics as both enhancement-mode types and JFETs. If you are familiar with using those devices, then dealing with depletion-mode MOSFETs will be straightforward. A few characteristics that may be a bit confusing are:

### 1. Drain saturation current - $I_{DSS}$

With an enhancement-mode MOSFET this is a leakage current. With a depletion-mode MOSFET it is the maximum limiting current that can flow between the drain and source, which occurs at a particular drain-to-source voltage ( $V_{DS}$ ), when the gate-to-source voltage is at zero ( $V_{GS} = 0$ ). This particular curve is depicted in all MOSFET data sheets, and is where the drain current increases linearly, then begins to be pinched-off at the knee of the curve. It is important to remember that  $I_{DSS}$  may typically range over 3:1 for similar devices. It is also temperature sensitive, and has a negative temperature coefficient of approximately  $-0.5\%/^{\circ}\text{C}$ .

### 2. Gate-to-source cutoff voltage $V_{GS(off)}$ and gate threshold voltage - $V_{TH}$

This is a bit confusing, because this is the key characteristic specifying the voltage necessary to turn the device OFF. Some manufacturers use the depletion-mode terminology  $V_{GS(off)}$ , while others use the more commonly understood  $V_{TH}$  which is a term used for enhancement-mode devices. They imply the same thing. For an N-channel device the gate-to-source voltage ( $V_{GS}$ ) ranges from 0V for full conduction, to some negative amount of several volts to turn it off. A P-channel device ranges from 0V for full conduction, to several positive volts to turn it off.

The applied voltage should be more than the specified value to ensure turn-off. The  $V_{GS(off)}$  "transfer" curve is depicted in most MOSFET data sheets, and is shown in **Figure 3**, and in **Table 1d**.  $V_{GS(off)}$  shifts with temperature, and has a negative temperature coefficient of approximately  $-2\text{mV}/^\circ\text{C}$ . While most manufacturers simply specify minimum/maximum values, Advanced Linear Devices guarantees precise gate thresholds as low as  $\pm 20\text{-mV}$  for their ultra-low voltage EPAD devices, and Infineon provide gate threshold voltages in  $200\text{-mV}$  steps for their devices.

## Applications

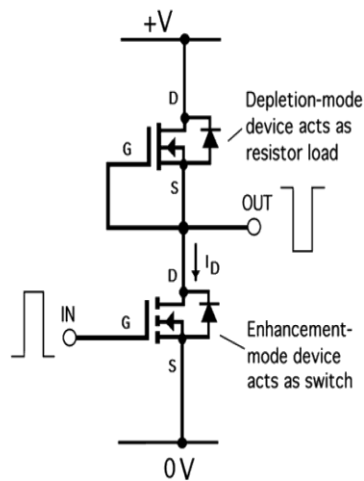
The depletion-mode MOSFET will function in those applications requiring a "normally-on" switch. This can be a very low voltage/current circuit which could use a matched dual or quad integrated circuit array from Advanced Linear Devices. A low or medium power circuit could use discrete device(s) from Supertex, Infineon, or Clare. If the application needed a high current (i.e. 5A), and/or high voltage ( $>250\text{V}$ ) normally-on switch, one could choose from various devices from IXYS. For low-voltage RF applications Philips Semiconductors offer specially designed depletion-mode MOSFETs for low-loss RF switching, up to 1GHz. **Table 2** provides a summary, and helpful contact information.

U.S. Manufacturers of Depletion-mode MOSFETs				
MANUFACTURER:	Description:	$BV_{DSX}$ Range:	$I_D$ MAX in Range:	Special Notes:
ADVANCED LINEAR DEVICES, INC. 415 Taiman Dr. Sunnyvale CA 94089-1706 Tel: (408) 747-1155 www.alinc.com	I.C. Ultra-low Power Matched Dual/Quad Arrays	$<10\text{V}$	$<20\text{mA}$	<ul style="list-style-type: none"> <li>Precision matched gate thresholds <math>\pm 20\text{mV}</math></li> <li>Ultra-low leakage</li> <li>Excellent temp. tracking</li> <li>DIP and SOIC</li> </ul>
CLARE, INC. 78 Cherry Hill Dr. Beverly MA 01915-1048 Tel: (978) 524-6700 www.clare.com	Discrete Low/Medium Power	$250\text{V} - 400\text{V}$	$300\text{mA}$	<ul style="list-style-type: none"> <li>Silicon-gate vertical DMOS</li> <li>High reliability</li> <li>Low <math>R_{DS(on)}</math> at cold temperatures</li> <li>SOT-89/223</li> </ul>
INFINEON TECHNOLOGIES 1730 N. First St. San Jose CA 95112 Tel: 1-866-951-9511 www.infineon.com	Discrete Low/Medium Power	$60\text{V} - 600\text{V}$	$140\text{mA}$	<ul style="list-style-type: none"> <li>SiPMOS<sup>®</sup></li> <li>Selected <math>V_{GS(TH)}</math> in 5 bands</li> <li>dv/dt rated</li> <li>SOT-23/223</li> </ul>
IXYS CORP. 2540 Bassett St. Santa Clara CA 95054 Tel: (408) 982-0700 www.ixys.com	Discrete Medium/High Power	$500\text{V} - 1\text{KV}$	$20\text{A}$	<ul style="list-style-type: none"> <li>Very rugged devices</li> <li><math>V_{OSS}</math> @ <math>500\text{V}/1\text{KV}</math></li> <li><math>I_{DS}</math> @ <math>25^\circ\text{C}</math>: <math>0.1\text{A} - 20\text{A}</math></li> <li>TO-220, 247, 251, TO-252, and 268</li> </ul>
PHILIPS SEMICONDUCTORS 811 E. Arques Ave. Sunnyvale CA 94088-3409 Tel: 1-800-234-7381 www.semiconductors.philips.com	Discrete Low Power RF	$<7\text{V}$	$<10\text{mA}$	<ul style="list-style-type: none"> <li>Specially designed for low-loss RF switching</li> <li>Up to 1-GHz</li> <li>Transceiver switching</li> <li>SOT-23, 143, 323</li> </ul>
SUPERTEX, INC. 1235 Bordeaux Dr. Sunnyvale CA 94089 Tel: (408) 222-8888 www.supertex.com	Discrete Low/Medium Power	$250\text{V} - 700\text{V}$	$0.5\text{A}$	<ul style="list-style-type: none"> <li>Silicon-gate vertical and lateral DMOS</li> <li>Low <math>V_{GS(TH)}</math></li> <li><math>V_{OSS}</math> @ <math>250 - 700\text{V}</math></li> <li>SOT-23/89, TO-92 and TO-220</li> </ul>

(Click to Enlarge Image)  
Table 2

Let's look at some diverse application examples for the depletion-mode device.

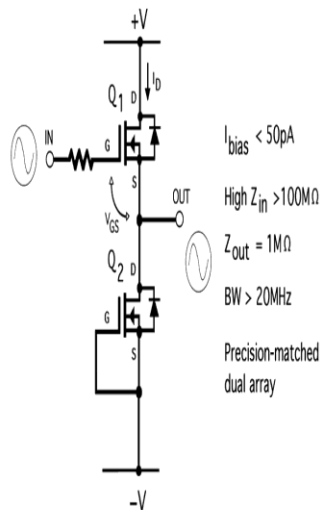
**Figure 4** shows how a typical inverter in NMOS logic used to be created by manufacturers. The depletion-mode transistor acts as a drain load resistor for the lower transistor (enhancement-mode), which functions as a switch. The resistor's value is created by ion-implantation.



A typical NMOS inverter where the depletion-mode device is used as a drain load for the enhancement-mode transistor.

(Click to Enlarge Image)  
Figure 4

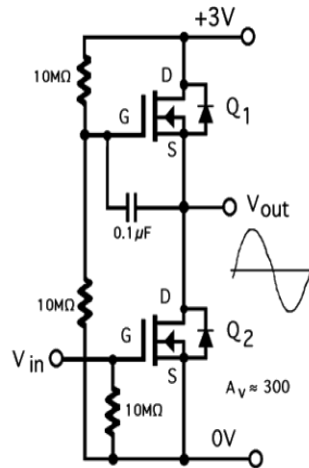
**Figure 5** shows how a simple voltage follower could be implemented using a matched pair of ALD depletion-mode devices. Because the MOS devices are matched, the initial offsets and their associated drifts are eliminated. The circuit provides very high input impedance and a very low input bias current.



A simple voltage follower implemented with a matched pair of depletion-mode MOSFETs.

(Click to Enlarge Image)  
Figure 5

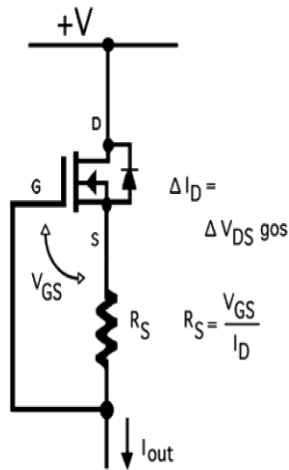
**Figure 6** depicts a simple high-gain, low-voltage (audio or sensor) cascode preamplifier which could be implemented using a matched pair of depletion-mode devices. The circuit could run with either lower- or higher-supply voltages, and provide very high input impedance.



A high-gain, low-voltage, cascode audio amplifier using matched dual depletion-mode MOSFETs.

*(Click to Enlarge Image)*  
Figure 6

**Figure 7** shows a simple self-regulating current source running at either a very low voltage (i.e. 3V), or at a very high voltage (i.e. >150V). Choose an appropriate device regards voltage rating, current rating ( $I_{DSS}$ ), and conductance (choose a low  $g_{os}$  value). Current regulation is enhanced by choosing a low current, such as <5% of the MOSFET's  $I_{DSS}$  rating. Regulation will then be about 1% or better.



### N-channel depletion-mode MOSFET current source

*(Click to Enlarge Image)*  
Figure 7

**Figure 8** shows another current source, but this time combining a voltage reference IC with the MOSFET, which compensates for supply voltage fluctuations. The current source provides a total current to the load ( $I_{LD}$ ), comprising the set current through the resistor ( $I_{SET}$ ), and the quiescent current from the reference ( $I_Q$ ). This circuit can provide a very high level of precision, and ultra-high output impedance.



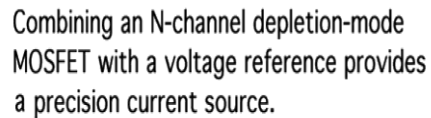


Figure 8

polypropylene type. Transistor  $Q_2$  acts as an output buffer, while amplifier  $A_2$  provides feedback.

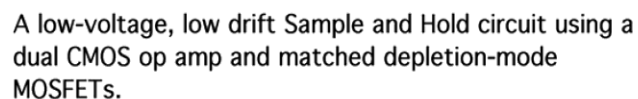
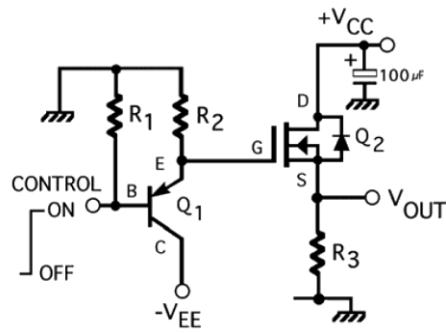


Figure 9

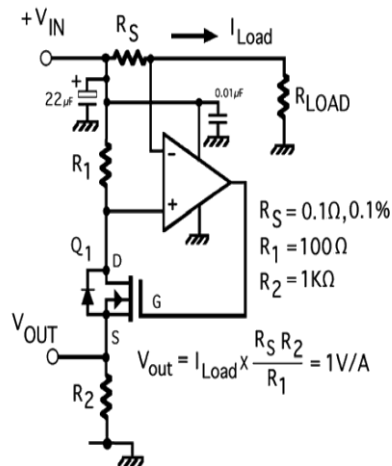
**Figure 10** shows a simple normally-on switch using a depletion-mode MOSFET. The PNP switches between 0V and  $-V_{EE}$  to provide the necessary gate bias for the MOSFET. With no control signal to the PNP, the MOSFET is conducting. A PNP is shown for simplicity.



Normally-on switch using a depletion-mode MOSFET

(Click to Enlarge Image)  
Figure 10

**Figure 11** shows a simple current monitor using an op amp and a depletion-mode MOSFET. Resistor  $R_1$  monitors the current to the load, and should be a quality 0.1% wirewound type with the appropriate wattage rating. The MOSFET provides an output voltage proportional to the current being monitored (in this example, one volt per amp), which could be displayed on a DVM, used to trigger a comparator, or input to an A/D converter.



Current monitor using a depletion-mode MOSFET and a single-supply op amp.

(Click to Enlarge Image)  
Figure 11

In summary the depletion-mode MOSFET can be uniquely applied in many diverse applications, and somewhat differently to the enhancement-mode type. The depletion-mode device is today receiving increased worldwide attention as the semiconductor industry looks for new innovative ways to provide even lower voltage operation and lower power solutions for tomorrow's designs.

Some researchers are looking at building depletion-mode MOSFETs with different materials, such as gallium arsenide (GaAs) or indium phosphide (InP), so as to create RF power amplifiers for next generation cellular communications. Others are looking at creating different depletion-mode structures, and at sub-threshold operation to provide even lower power solutions. They say, "you can't teach an old dog new tricks", but if you take a fresh look at these devices, you'll find they offer the only answers for which designers are looking.

**About the author**

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